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Advancements in Low-power Digital Circuitry: A Comparative Survey

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Abstract*— In order to identify recent developments in low-power digital circuits, this literature review conducts an exhaustive search. Among the many topics covered by these books and journals is a comprehensive examination of some of the most fundamental components of digital electronics, such as Johnson counters, binary counters, shift-and-add multipliers, and low-power multipliers based on Universal Shift Registers (USR). The findings of this study offer novel strategies for reducing digital system energy consumption, enhancing circuit efficiency, and creating greener computing environments. The methods discussed, which include transistor gating, symmetric stacking, and enhanced USR-based designs, have the potential to substantially reduce power consumption. The incorporation of energy-efficient digital electronics into established industries such as mobile computing, the Internet of Things (IoT), and battery-dependent products is likely to increase their prevalence. This review's emphasis on the role of power management techniques in influencing the future of digital circuit design may result in more energy-efficient and cost-effective electronics.

***Index Terms*— Johnson Counter, Internet of Things (IoT), Universal Shift Register (USR), Three-bit stacker circuit, Multiplier.**

I. INTRODUCTION

Digital electronics permeate every aspect of the existence in the world of today's swiftly advancing technology [1]. Smartphones, laptops, smart appliances, and industrial automation, to name a few, rely on digital circuits in order to function. The relentless pursuit of innovation in the digital realm has resulted in an expansion of processing power and features, but with this development have come concerns regarding the concomitant increase in energy consumption [2]. As this continues to integrate digital technology into formerly analog domains, there has never been a greater need for eco-friendly, energy-efficient electronic devices [3]. This study sets out to investigate recent advancements in low-power digital circuitry. The discussion centers on five research papers that each take a unique approach to the age-old problem of the limited battery lifetimes of digital devices [4]. These works examine numerous elementary digital building blocks, such as Johnson counters, binary counters, shift-and-add multipliers, and low-power multiplier designs based on Universal Shift Registers (USR). This sheds light on these studies so as to better comprehend their outcomes, methodologies, and most importantly, their impact on the development of low-power digital devices [5].

This investigation cannot be conducted without the Johnson counter. Despite its widespread use in data transit and logic design, this digital circuit has been plagued by excessive energy consumption for a long time [6]. The first paper presents a novel strategy for creating a power-efficient Johnson counter using transistor gating. This innovation may revolutionize the digital circuit industry by enabling the construction of low-power circuitry without sacrificing performance. This work breaks new ground by shedding light on the possibility of significant energy reductions in a fundamental component of digital systems [7]. There are two main defects in the traditional binary counter: gate proliferation and carry propagation latency. The second paper this examines introduces an original technique known as symmetric stacking, which has the potential to eradicate carry propagation completely [8]. This inventive design employs carry-save adders to simplify the underlying circuitry and increase counting efficiency. The findings of this study demonstrate the revolutionary potential of this approach for binary counters, paving the way for the design of digital circuits that are more efficient and consume less energy [9].

Low-power multipliers, crucial components of modern computers, are discussed in the third paper. In this paper, this presents a novel method for designing low-power multipliers based on a customized Universal Shift Register (USR) [10]. This architecture prioritizes left shift and Load operations to reduce energy consumption, space requirements, and latency in comparison to conventional installations. The USR is ideal for this mission due to its adaptability, as it can be utilized in a multitude of ways depending on the selected mode. Extensive simulations and real-world testing supported the benefits of this low-power multiplier design in this study. When this delves deeper into these findings, this discovers a promising new way to improve the efficacy of digital computation [11]. A novel viewpoint on Johnson counters, highlighting their excessive energy consumption. This study recommends using Gate Diffusion Input (GDI) logic gates because they are more efficient and require fewer transistors than D flip-flops, which are traditionally used in Johnson counters. This research devised innovative XOR, XNOR, and NAND gates that consume significantly less power than conventional D flip-flops. Utilizing low-power J-K flip-flops

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in toggle mode is another strategy for reducing power consumption. A flip-flop design that considerably reduces power consumption by replacing conventional OR gates with AND gates using pass transistor logic (PTL) is a notable innovation. The study suggests using a technique known as "clock gating" to turn off portions of a circuit that are not in use in order to further reduce power consumption. The findings indicate that the technique has the potential to significantly reduce power consumption, making it a viable option for low-power digital circuitry. These studies illuminate the significance of power management strategies in the design of cutting-edge digital circuits and the never-ending pursuit for low-power digital electronics. As this distribute this survey, this will gain insight into how these developments may influence the future of energy-efficient, environmentally favorable digital systems. This hopes that digital technology and energy efficiency can coexist in the future, and the research will illuminate the path to that future.

II. PROPOSED WORK

According to Ajay Kumar et al [12] proposed that when designing environmentally friendly, energy-efficient digital electronics, power consumption must be considered. Johnson counters are an integral part of digital electronics, from data transfer to logic design. However, their inordinate energy consumption has been a problem. Using a transistor gating mechanism to create a Johnson counter that consumes very little power, this paper offers a novel solution to this problem. The versatility of the Johnson counter as a pulse counter makes it an indispensable part of digital electronics. It simulates the operation of a shift register by cycling data through its many phases continuously. This quality makes it applicable to multiple logic designs. Before diving headfirst into the suggested approach, it is essential to have a solid comprehension of the necessary concepts. A crucial type of counter, the ring counter comprises of a series of flip-flops. The D flip-flop is a crucial component of digital circuitry that can store a single bit of data and transition between two states. This research provides a comprehensive analysis of these components, which is essential for understanding the proposed solution. The Johnson counter must utilize a transistor gating mechanism for the proposed repair to be effective. This technique conserves a great deal of energy because it utilizes transistors to regulate the passage of current in a circuit. When the device is turned off, two slumber transistors strategically positioned in the circuit halt the flow of electricity. Adding these slumber transistors to the Johnson counter is necessary to maximize its efficacy. This study's primary objective was to identify a method for reducing the power requirements of a 4-bit Johnson counter, and the results are optimistic in this regard. The current Johnson counter consumes 2.101739e-003 watts of energy. Utilizing the proposed transistor-gated D flip-flop and NAND gate reduces power consumption to 1.0980e-005 watts. This drastically diminished energy consumption is evidence that the proposed method is effective. The proposed Johnson counter's energy consumption is just 5.738886e-004 watts, which is a significant improvement over the current Johnson counter. This study concludes with a novel method for resolving the power limitations of Johnson counters. The proposed method relies heavily on sleep transistors and a transistor gating system to reduce power consumption by a significant margin. In light of these findings, the proposed Johnson counter is a viable option for the development of low-power digital circuitry. This study highlights the importance of power management strategies in the swiftly evolving digital ecosystem of today. This contributes to the development of electronic systems that are friendlier to the environment and more durable over time by minimizing the power requirements of critical components such as Johnson counters. The findings of this study pave the way for advancements in the design of low-power digital circuits, which may have far-reaching effects across numerous industries and applications. Fig 1 depicts the Johnson counters.

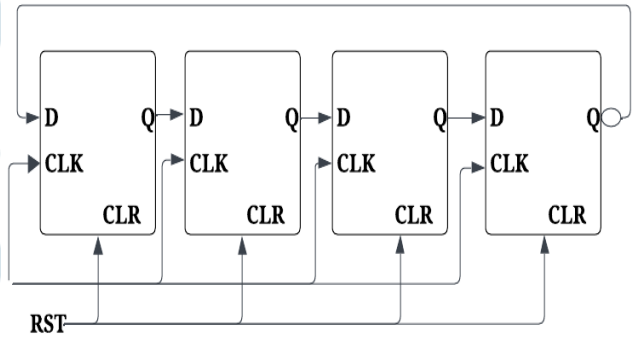

Fig. 1. Johnson Counter

C. Fritz et al [13] proposed that digital electronics, binary counters are indispensable for a variety of counting and sequencing applications. However, traditional binary counters have been plagued by issues such as the need for multiple gates and the inherent latency caused by carry propagation for quite some time. Using a standard binary counter has its limitations. They frequently require a large quantity of gates, which can increase design complexity and delay signal transmission. Carry propagation latency may considerably constrain the overall efficacy of such devices. The proposed design is revolutionary because it introduces symmetric stacking to the world of binary counters. This new technique entails superimposing two similar circuits with their outputs connected in series to the inputs of the underlying circuit. By eliminating the requirement for carry propagation, this effectively resolves a significant problem with conventional binary counters. This uses a combination of carry-save adders and compressors to further enhance the speed and efficacy of the design. These components improve the counting procedure while decreasing the number of required gates. For your convenience, the design is fully

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explained with a circuit diagram and logic calculations. Comparing the efficacy of the design to that of other common binary counters demonstrates that it is superior. The results conclusively demonstrate that the design is more efficient and contains fewer gates than its competitors. This comparison highlights the potential game-changing nature of the approach to binary counters. The analysis demonstrates that the layout proposal is superior. This demonstrates the commitment to developing innovative computer systems. Compared to conventional counters, the innovation significantly improves their efficiency and usability. Using simulations with a 32-bit binary counter, this demonstrates that the design is functional. The results of the simulation are astounding. This innovation's utmost frequency is 1.5 GHz, which is significantly higher than anything else on the market. The design is not only more efficient than rival models, it also consumes less energy. This proposed study design for binary counters that addresses the shortcomings of existing solutions. This symmetric stacking architecture eliminates a significant impediment in conventional binary counters, the elimination of carrier propagation. Utilizing carry-save adders and compressors significantly improves the design's speed and efficiency. Fig 2 depicts the three-bit stacker circuit.

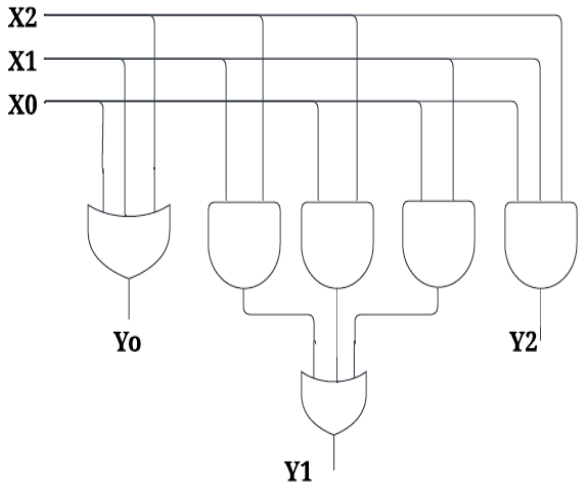

Fig. 2. Three-bit stacker circuit.

S. P. Valan Arasu et al [14] proposed that the utmost feasible level of power efficiency in the design of digital circuitry should be a top priority. As the use of electronic devices becomes more prevalent in the daily lives, it is becoming more important than ever to aspire for reduced space and power consumption in circuit designs. In this research paper, a low-power multiplier design based on a modified Universal Shift Register (USR) is proposed as an innovative solution to this problem. This methodology is presented as a low-power multiplier. This new design is significantly optimized for left shift and Load operations, resulting in a significant reduction in power consumption, space requirements, and delay in comparison to conventional systems. This is because the updated architecture is optimized for left shift and Load operations in particular. The Universal Shift Register, or USR for short, is a component in digital circuitry that is renowned for its versatility due to its ability to perform a variety of duties based on the mode that is selected for it. This ability enables its use in a variety of applications. Users of the USR generally have the option of selecting one of four unique modes of operation, with the mode they choose being determined by the parameters of M0 and M1. When M0M1 equals 00, the USR functions as a data transfer register, cycling output into input. When the USR is in the reset state, this occurs. When M0M1 is set to 01, shift operations are performed to the left, whereas when M0M1 is set to 10, shift operations are performed to the right. When M0M1 equals 11, input data is fed into the register in parallel. This is the final stage, but it is still crucial. In this investigation, a novel construction strategy for the USR has been presented. The primary objective is to reduce power consumption while simultaneously performing a predetermined set of actions, namely left shift and Load. By refining the circuitry, this improved USR design reduces power consumption while maintaining the same level of efficacy. Figure 4 depicts the design that has been recommended, which consists of a mode selector line depicted by the letter 'S' for the purpose of selecting the appropriate mode of operation. To determine whether or not the proposed revised USR-based low-power multiplier architecture is effective, a large number of simulations utilizing the extensive capabilities of Xilinx ISE 14.2 were performed. In order to conduct a realistic evaluation, the architecture was additionally implemented on a Spartan 3E field-programmable gate array (FPGA). The simulation results provide compelling evidence of the benefits that can be realized by implementing the suggested design. Two main categories of conclusions can be drawn from the results of the recommended research. To begin with, the novel architecture based on USR consumes significantly less energy and has a smaller footprint compared to conventional designs. This is an extremely useful feature, especially for energy-conscious applications and battery-powered devices. Second, the proposed design substantially reduces the amount of latency, which contributes to the quicker and more responsive functionality of the circuitry. This architecture is an attractive solution for applications where speed is of the utmost importance, as it considerably reduces the amount of latency that the system experiences. Modifications to the Universal Shift Register (USR) are proposed as a ground-breaking strategy for the construction of low-power multipliers, as suggested in the study's conclusion. To effectively execute this endeavor, a specialized shift register was employed. The proposed configuration not only reduces the amount of power used and the amount of space required, but it also reduces the amount of delay that is produced as a consequence. This is accomplished by placing a greater emphasis on left-shift and

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Volume 11 Issue 3 March 2024

load activities and by providing a simplified mode option. The findings position the modified USR-based architecture to be an attractive alternative for a variety of applications requiring designs that consume less energy and are more compact. The necessity for these characteristics necessitates these designs. If confirmed, the results of this investigation will have a wide range of consequences. It may be advantageous to industries such as mobile computing, the Internet of Things (IoT), and other battery-reliant devices due to its potential to improve overall energy efficiency and prolong battery life. This is due to the fact that it can extend the lifespan of batteries. Because integrated circuits require less space, it is conceivable that they can be manufactured at a lower cost. Fig 3 depicts the block diagram of multiplier.

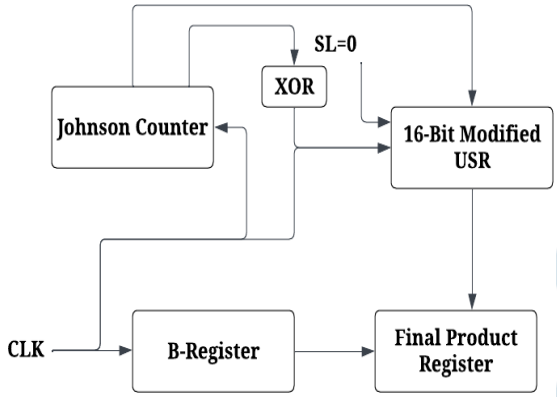

Fig. 3. Multiplier block diagram

S. Asif et al [15] that in the design of digital circuits, the search for quick and effective arithmetic processing continues. The purpose of this paper is to provide a novel design for rapid arithmetic circuits to address this problem. This design is based on a combination of techniques that optimize the benefits of CMOS 4-2 and 5-2 compressors, multi-input counter and compressor circuits, and enhanced final adders. The end result is a high-performance system with the potential to increase computing speed and efficiency. The first section of the paper is a comprehensive literature review on rapid arithmetic circuits. The literature review on high-speed multiplier design and area-efficient VLSI adders provides the foundation for the novel method presented here. This exhaustive analysis of previous efforts does more than simply give credit where credit is due; it also identifies faults and provides recommendations for moving forward. This research focuses on a configuration proposal for high-speed arithmetic circuits. Utilized is an interdisciplinary strategy that incorporates numerous approaches and resources. CMOS technology is used to implement the 4-2 and 5-2 compressors, the parallel prefix computation, the multi-input counter and compressor circuits, and the meticulously constructed final adders. This architecture relies significantly on the parallel prefix computation technique, which accelerates arithmetic operations by leveraging parallelism. By dividing labor-intensive computations into more manageable parallel phases, this method dramatically increases both speed and productivity. CMOS 4-2 and 5-2 compressors are used to demonstrate the design's attention to detail. This type of compressor is essential for reducing data size and facilitating calculation speed increases. The proposed architecture employs multi-input counter and compressor circuits to enhance the data processing efficiency. This technique reduces the time required for data to travel between nodes, thereby enabling quicker calculations. To ensure that all components of the design contribute to speed and efficiency, the essay explores the topic of final adders that have been optimized. Here, the arithmetic circuits are optimized for lightning-fast calculations. Comprehensive simulations and exhaustive comparisons with other designs validate the efficacy of the proposed method. In the context of low-power circuit design, comparisons of power consumption versus performance and area efficiency are crucial. The simulation results indicate that the proposed method is more effective and requires less space than the alternatives. By meticulously integrating parallelism, CMOS compressors, multi-input circuits, and enhanced adders, a state-of-the-art arithmetic solution was realized. In addition to a comprehensive analysis of power consumption, the paper demonstrates that the proposed design is competitive with other options. The increased emphasis on low power consumption in contemporary electronic devices makes this a significant finding. This research proposes a revolutionary architecture for high-speed arithmetic circuits using CMOS 4-2 and 5-2 compressors, parallel prefix computation, multi-input counter and compressor circuits, and improved final adders. The proposed configuration has been determined to be the most efficient in terms of speed, footprint, and energy consumption after a comparison of numerous alternatives.

P. S. Rana et al [16] proposed that Johnson counters are digital circuits whose output sequence repeats after a predetermined number of cycles. Traditional Johnson counters have utilized D flip-flops, which are notorious for their high -power consumption. To modernize this concept, the proposed design employs GDI logic gates, which are known for their low power consumption and lesser transistor count. Gate Diffusion Input (GDI) logic gates are an effective instrument for the construction of low-power digital circuits. The logic operations of these gates are managed by diffusion current, which reduces power consumption and transistor count. Compared to conventional D flip-flops, the XOR, XNOR, and NAND gates used in the design's 4-bit flip-flop considerably reduce power consumption. To further enhance power efficiency, the proposed design includes low-power J-K flip-flops operating in toggle mode. Power is conserved by maintaining the J and K terminals in the active high position. The most significant enhancement, however, is a new flip-flop design that utilizes even less energy than its predecessors. The charging and discharging of the transistors

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Volume 11 Issue 3 March 2024

in this flip-flop are controlled by a pass transistor logic (PTL)-based AND gate instead of conventional logic gates. This indicates that the output node requires very little energy to function. This study introduces a novel concept known as "clock gating," which has been demonstrated to further reduce energy consumption. Clock gating is an established method for isolating the clock signal from unused circuit components. Clock gating is implemented to disable the flip-flops' clock signal when they are not in use. Extensive tests were conducted between 600 MHz and 1 GHz to evaluate the performance of the proposed system. To determine the quantity of energy saved, the power consumption was measured in microwatts (W). The results conclusively demonstrate that the proposed architecture is preferable to the existing one. At 800 MHz, compared to the industry standard of 5.93 W, the proposed architecture only consumes 4.88 W of power. At 1000 MHz, the proposed design is still superior, with a power consumption of 4.39 W versus 7.31 W for the conventional alternative. These results demonstrate that the proposed design is extremely power-efficient, making it optimal for use in environments with limited power. This study introduces a novel low-power Johnson counter hardware solution by integrating GDI logic gates with clock gating techniques. Compared to the status quo, the proposed arrangement could reduce energy consumption by as much as 68.18 percent. Depending on the frequency, clock gating, a method for improving energy efficiency, can reduce power consumption by between 37.12% and 41.08%. The findings of this research provide optimism for the future of low-power digital circuit design.

III. RESULTS

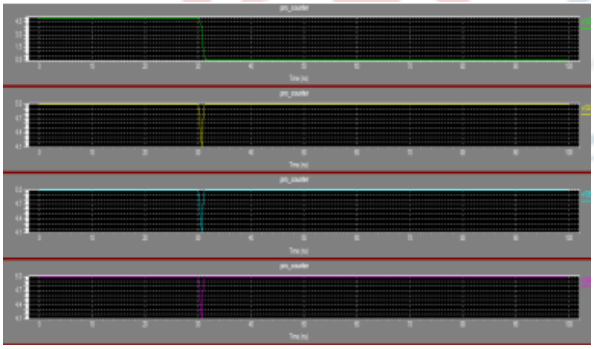

Fig. 4. Johnson Counter Waveform

Table 1. Comparison of all methods

	Power Consumption
Johnson Counters [12]	5.738886e-004 watts
Binary Counters [13]	5.5e-0.03 W
Shift & Add Multiplier [14]	172 mW
Counter Based Wallace [15]	6.04 nW
Johnson Counters [16]	11.96e-0.06 watts

Fig 4 depicts the Johnson counter waveform. A comparison of multiple designs for low-power digital circuitry may shed light on the topic of power efficiency as shown in Table 1 and Fig 5. By utilizing a transistor gating mechanism [12], the power consumption of Johnson counters was drastically reduced. With the proposed design, power consumption falls from 5.738886e-004 watts to 1.0980e-05 watts, a substantial improvement in energy efficiency. With the advent of symmetric stacking [13], binary counters have taken an optimistic stride forward. The fact that problems with gate proliferation and carrier propagation delay have been resolved is indicative of increased efficiency, but the graph does not include information on power consumption. With a power consumption of just 172 mW, the Universal Shift Register (USR)-based multiplier design in Reference 14 demonstrates significant progress in reducing the power requirements of digital multipliers. Multiplication is more efficient due to the design's capacity for left shift and Load optimization. Using a counter, Wallace's [15] technique reduces power consumption to a remarkable 6.04 nW. This is a significant advancement in the search for low-power digital circuitry and may have far-reaching implications for the future of many energy-efficient technologies. Utilizing clock gating techniques and Gate Diffusion Input (GDI) logic gates, Johnson counters [16] are able to considerably reduce their power consumption. Their proposed architecture consumes only 11.96e-0.06 watts of energy, making it a competitive method for achieving energy-efficient digital circuitry.

The "Counter Based Wallace" method by S. Asif et al. uses the least energy (6.04 nW) of all the methods are examined. This method has great potential for applications in which minimizing power consumption is crucial.

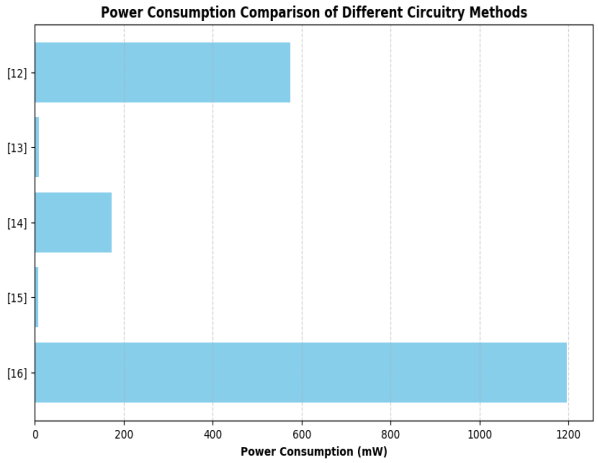

Fig. 5. Power Consumption comparison

IV. CONCLUSION

Recent research on low-power digital circuits has revealed a promising new direction for the development of eco-friendly and low-energy digital products. By examining

these five studies, shows how the problem of high-power consumption in essential digital components can be addressed in novel ways. These studies have revealed substantial opportunities for energy savings without sacrificing functionality, especially through novel concepts such as symmetric stacking in binary counters and the reconstruction of Johnson counters with transistor gating. Utilizing a modified Universal Shift Register (USR) in low-power multiplier architectures has led to increased efficiency, decreased power consumption, and decreased latency. In addition, the use of Gate Diffusion Input (GDI) logic gates and clock gating techniques has ushered in a new era of energy efficiency for Johnson counters. Considered as a whole, these results indicate that power management techniques will likely play a significant role in influencing the future of digital circuit design. The most recent developments, as outlined below, hold the promise of more resilient and cost-effective electronic systems with a variety of potential applications. These developments provide insight into how digital technology and energy efficiency may coexist in the future.

REFERENCES

[1] X. Wu and Massoud Pedram, "Low power sequential circuit design using priority encoding and clock gating", Power Electronics and Design, 2000. ISLPED '00. Proceedings of the 2000 International Symposium on, 143-148, July 2000.

[2] X. Wu, J. Wei and M. Pedram, "Low-power design of sequential circuits using a quasi-synchronous derived clock", in Proc. Of ASP-DAC, Pacifico Yokohama, January 2000.

[3] G. Bhargave, S. Uniyal and P. Sheokand, "Low power adiabatic 4-Bit Johnson counter based on power-gating CPAL logic," 2016 Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH), Ghaziabad, India, 2016, pp. 297-301.

[4] F. Fallah and M. Pedram, "Standby and Active Leakage Current Control and Minimization in CMOS VLSI Circuits", IEICE Transactions on Electronics, vol. E88, no. 4, pp. 509-519, 2005.

[5] F. Fallah and M. Pedram, "Standby and Active Leakage Current Control and Minimization in CMOS VLSI Circuits", IEICE Transactions on Electronics, vol. E88, no. 4, pp. 509-519, 2005.

[6] Hu Jianping, Xu Tiefeng, Yu Junjun and Xia Yinshui, "Low Power Dual Transmission Gate Adiabatic Logic Circuits and Design of SRAM", Proc. IEEE MWSCAS'04, pp. 565-568, 2004.

[7] S. M. Ismail, A. B. M. S. Rahman and F. T. Islam, "Low power design of Johnson Counter using clock gating," 2012 15th International Conference on Computer and Information Technology (ICCIT), Chittagong, Bangladesh, 2012, pp. 510-517.

[8] S. Asif and Y. Kong, "Design of an algorithmic wallace multiplier using high speed counters", Proc. IEEE Comput. Eng. Syst. (ICCES), pp. 133-138, Dec. 2015.

[9] S. Veeramachaneni, L. Avinash, M. Krishna and M. B. Srinivas, "Novel architectures for efficient (m n) parallel counters", Proc. 17th ACM Great Lakes Symp. VLSI, pp. 188-191, 2007.

[10] J. Gu and C.-H. Chang, "Low voltage low power (5:2) compressor cell for fast arithmetic circuits", Proc. IEEE Int. Conf. Acoust. Speech Signal Process. (ICASSP), vol. 2, pp. 661-664, Apr. 2003.

[11] M. Mehta, V. Parmar and E. Swartzlander, "High-speed multiplier design using multi-input counter and compressor circuits," [1991] Proceedings 10th IEEE Symposium on Computer Arithmetic, Grenoble, France, 1991, pp. 43-50.

[12] Kumar, A. (2021). Low power consumption-based Johnson counter by transistor gating technique. International Journal of Innovative Science and Research Technology, 4(3), 1-5.

[13] C. Fritz and A. T. Fam, "Fast Binary Counters Based on Symmetric Stacking," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 10, pp. 2971-2975, Oct. 2017.

[14] Arasu, S. P. Valan et al. “MODIFIED UNIVERSAL SHIFT REGISTER BASED LOW POWER MULTIPLIER ARCHITECTURE.” (2014).

[15] S. Asif and Y. Kong, "Design of an algorithmic Wallace multiplier using high speed counters," 2015 Tenth International Conference on Computer Engineering & Systems (ICCES), Cairo, Egypt, 2015, pp. 133-138.

[16] P. S. Rana "Design and Analysis of Low Power GDI Based Johnson Counter." International Journal of Scientific Research and Engineering Development, vol. 3, no. 1, Jan-Feb 2020, pp. 282-283.